# PATENT ABSTRACTS OF JAPAN

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## (54) CMOS DELAY CIRCUIT

(57)Abstract:

PURPOSE: To adjust a delicate delay time by inserting n-set of transfer gates having an on-resistance in parallel with a series resistance determining the delay time.

CONSTITUTION: N-set of transfer gates 41-4n are connected in parallel with a series resistor 3 in the CMOS delay circuit. For example, the resistance of the series resistor 3 and the resistance of the transfer gates 41-4n are all selected to be R and the delay time when the transfer gates 41-4n are all turned off, that is, when the combined resistance RT is R is selected to be γ0, then the delay time γ1 of the signal S1 is (τ0/2) when any of the transfer gates is turned on. Thus, the number of closed transfer gates 41-4n is controlled to adjust the delay time in more minute step.